NVMdurance Aviator

Solving one of the biggest challenges of 3D NAND deployment

NVMdurance Aviator enables deployment of 3D NAND flash in the most challenging applications. Manufacturers and users of NAND wish to transition to 3D NAND which can provide cost and performance advantages over 2D NAND, but there are many challenges for getting 3D NAND solutions to market.

NVMdurance Aviator uses proprietary machine learning technology from NVMdurance to automate the process of characterizing 3D NAND and provide the critical error management building blocks that require deep flash characterization and the ability to optimize around customer usage conditions.

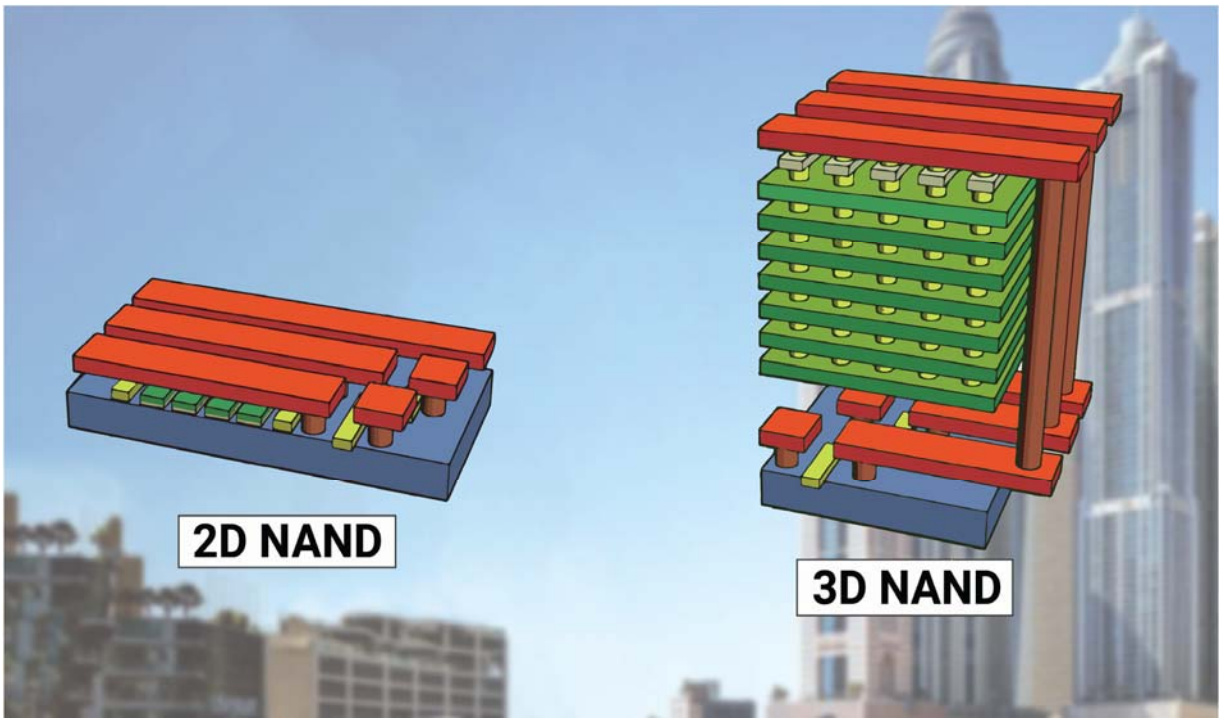
NVMdurance Aviator helps solution providers get to market faster and differentiate their products.

Background

Today, NAND flash memory is used to store data in many applications, including solid-state drives (SSDs), mobile phones, tablets, USB drives, memory cards, all-flash arrays and storage appliances. A type of NAND technology, called 2D or planar NAND, has been used since its inception 30 years ago. 2D NAND has enabled many new applications over the years through cost reductions by scaling (reducing) the lithography used to manufacture the flash. For example, in the last 10 years, NAND process technologies have scaled from around 70 nanometers (nm) to where they are today in the 15nm range, following or even beating what Moore's Law would predict. Scaling is what provides density increases and cost per gigabyte (GB) reductions, enabling many new applications for NAND. 2D NAND is reaching the end of its physical and practical scaling limits, and a new technology is required to continue to provide density increases and cost per GB reductions.

This is exactly the problem that 3D NAND promises to solve. With 2D NAND, the cells that store individual bits of data are arranged in a planar manner, which is commonly referred to as the X-Y dimensions. 2D NAND cells are simply getting too close together to continue reducing the X-Y dimensions. 3D NAND technology solves this problem by arranging the

cells vertically, such that cost reductions happen by adding more cells in the vertical (Z) direction, commonly called the layer count. 3D NAND technologies in production today have 32 or 48 layers, and higher layer counts are in development. The figure below helps illustrate this.



Using a building analogy to represent the arrangement of the flash storage cells, one can imagine 2D NAND as a single-story building and scaling as adding more people within the same amount of space. Adding more people is analogous to increasing flash density and reducing cost per GB. We have reached the point where we cannot add more people with 2D NAND. On the other hand, 3D NAND is represented by a high-rise building, where more people can be added by adding more floors.

In addition to whether the flash uses 2D or 3D technology, the number of bits stored per flash cell also impacts the flash chip density and cost per GB, at the expense of reliability. The table below reflects this.

Acronym	Definition	Bits per Cell	Relative Cost per GB	Relative Reliability and Performance
SLC	Single-Level Cell	1	Highest	Highest
MLC	Multi-Level Cell	2	Medium	Medium
TLC	Triple-Level Cell	3	Lowest	Lowest

To maximize capacities and minimize cost per GB, 3D TLC is becoming the NAND flash of choice. However, there are many challenges in replacing 2D with 3D TLC NAND and realizing all of the benefits.

3D NAND deployment challenges

One of the biggest technical challenges with introducing new NAND technologies is managing the errors that are inherent with NAND. Every NAND flash technology, meaning a specific manufacturer's lithography or layer count, has a certain Raw Bit Error Rate (RBER), which is the rate that the flash chip produces errors. As flash is scaled or layer count increases, the RBER increases. Additionally, as a flash chip ages in the application, which means the more it is written to, read from, erased or even sitting idle storing data, the RBER increases. This increasing error rate is exacerbated with 3D NAND due to the introduction of the vertical (Z) direction and the cell-to-cell interference that causes. Another critical factor is the number of bits per cell. The RBER for TLC is significantly higher than for MLC NAND, even within the same lithography or layer count. Referring to the table above, the lowest cost, highest density NAND solutions (TLC) also have the highest RBER or lowest inherent reliability.

To correct the vast majority of these errors and provide an acceptable error rate in the system, all NAND flash applications utilize controllers with Error Correction Code (ECC) schemes. ECC uses extra bits of information that are tied to the actual data being read to determine if there is an error in the data and correct it. The ECC requirement depends on the flash technology and the reliability requirements of the application. The flash manufacturers specify the ECC requirements for their individual flash devices, and it is up to the solution provider to select a controller that provides sufficient ECC capability for their

application. Many chose to deploy “off-the-shelf” flash controllers from controller suppliers, but some develop their own controllers, typically integrated into a larger chip that performs other functions, such as an ASIC or FPGA. Whomever develops the controller must determine what type of flash they will support and provide sufficient ECC capability for the intended application.

For 2D NAND, a type of ECC called BCH (the acronym BCH comprises the initials of the three inventors’ surnames) is the most commonly utilized today. BCH and other ECC methods used for 2D NAND have what is commonly called “hard data” detection and correction schemes, meaning the extra bits of information that come along with the data are used to definitively detect errors in the data. The decision is “hard” since there is either an error detected and corrected in the data or there is not. BCH has been around for decades and is relatively easy to deploy. Many 2D NAND solution providers can purchase “off-the-shelf” controllers that have BCH ECC engines and all of the necessary firmware to deploy their solution utilizing the latest 2D NAND technologies.

3D NAND, in particular 3D TLC, makes this much more complex, because traditional ECC methods can no longer be utilized and “off-the-shelf” solutions are scarce. LDPC (Low Density Parity Check) and other advanced ECC methods required for 3D NAND, supplement the hard data detection with “soft data” information, based on a fundamental understanding of how the NAND flash actually behaves, in order to correct errors in the data that purely hard data detection and correction methods cannot handle. In order to properly decode the soft data and determine the probability of errors and correct them if necessary, some critical tools to aid the ECC engine are required, including Log-Likelihood-Ratio (LLR) tables and error models. Developing these tools requires a deep, up-front characterization of the flash, prior to deployment in a system, and the ability to translate the flash behavior into application-specific solutions.

Because of the complexity of LDPC and other soft-data ECC methods, 3D NAND is much more challenging to deploy in a system. As a result, there are very few “off-the-shelf” solutions available, especially for those who want to deploy 3D TLC in high-performance, high-reliability applications, such as datacenter and enterprise SSDs, and optimize for different use cases and applications. Additionally, these soft-data ECC methods, require a deep characterization of the flash memory technology prior to deployment of the solution.

In summary, solution providers looking to deploy 3D NAND in their application need to find solutions that can reliability predict and correct errors, and to do so requires a deep characterization of the flash technology being deployed, as well as the ability to translate the characterization data into application-specific solutions. Up to now, 3D NAND characterization has been a very manual, time-consuming process that very few companies have the resources and expertise to do.

The solution - NVMdurance Aviator

NVMdurance Aviator provides tools, including LLR tables and error models, necessary to deploy 3D TLC NAND in the toughest applications, and it allows our customers to optimize the flash endurance and data retention based upon their usage conditions and differentiate their solutions.

NVMdurance Aviator is based on patented and proprietary machine learning technology from NVMdurance, the world's only automated method of characterizing flash. This eliminates the requirement for solution providers to perform deep flash characterization themselves, reducing their cost and time-to-market with new 3D NAND solutions.
3D NAND flash is the future of NAND and promises to enable even more applications and disruption within the storage industry. However, there are many challenges in getting 3D NAND, especially TLC, to meet the requirements of high-performance, high-reliability applications, such as datacenter and enterprise SSDs. NVMdurance has solved one of the biggest challenges of deploying 3D NAND with NVMdurance Aviator.

Read more on the NVMdurance website:
https://www.nvmdurance.com/nvmdurance-software/aviator/